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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/781,330	02/18/2004	Hideki Hirayama	10449-079001 / PIS2003324	9450
26161	7590	12/07/2006	EXAMINER	
FISH & RICHARDSON PC P.O. BOX 1022 MINNEAPOLIS, MN 55440-1022			RIVERO, MINERVA	
			ART UNIT	PAPER NUMBER

2627

DATE MAILED: 12/07/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/781,330

Applicant(s)

HIRAYAMA ET AL.

Examiner

Minerva Rivero

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 18 February 2004.
- 2a) ☐ This action is FINAL. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-13 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-13 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 18 February 2004 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO/SB/08)
Paper No(s)/Mail Date _____
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date _____
- 5) ☐ Notice of Informal Patent Application
- 6) ☐ Other: _____

DETAILED ACTION

Priority

1. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1-6, and 11-12 are rejected under 35 U.S.C. 102(e) as being anticipated by Minamino *et al.* (US 6,657,929), hereinafter Minamino.

4. Regarding claim 1, Minamino discloses a clock generating device for generating a clock signal synchronizing with a wobble signal, which includes address information for a predetermined period, the clock generating device comprising:

a PLL circuit for generating an oscillation signal in accordance with the difference between the phase of a wobble signal and the phase of a clock signal and for generating the clock signal by synchronizing the oscillation signal with the wobble signal (Col. 8, Lines 45-57); and

a detection circuit, connected to the PLL circuit, for monitoring the wobble signal, detecting the predetermined period of the wobble signal that includes the address information, and holding the output of the PLL circuit in accordance with the detection (*wobble detection circuit and predetermined value t_1* , Col. 8, Lines 54-58).

5. Regarding claim 2, Minamino discloses a hold signal generator for generating a first hold signal that holds the output of the PLL circuit during a first period in accordance with the detection, and a second hold signal that holds the output of the PLL circuit during a second period in accordance with the detection, which differs from the first period (*low-level and high-level hold signal*, Col. 17, Lines 10-37); and

a signal selector, connected to the hold signal generator, for providing the PLL circuit with either one of the first and second hold signals (Col. 17, Lines 38-42).

6. Regarding claim 3, Minamino discloses the first period is shorter than the predetermined period, and the second period is longer than the predetermined period (*hold signal is kept at low level before clock count exceeds t_1 and at high level when it exceeds t_1* , Col. 17, Lines 10-37).

7. Regarding claim 4, Minamino discloses the cycle of the wobble signal changes with at least two timings in accordance with the address information of the predetermined period, and the hold signal generator generates a first hold signal for holding the output of the PLL circuit during a period between a first timing and a second timing, at which the cycle of the wobble signal changes (Col. 17, Lines 38-42).

8. Regarding claim 5, Minamino discloses the cycle of the wobble signal changes during the predetermined period, and the hold signal generator generates the second hold signal for holding the output of the PLL circuit during the second period, which is longer than the first period of the first hold signal, from a timing at which the cycle of the wobble signal changes (Col. 17, Lines 10-37).

9. Regarding claims 6 and 12, Minamino discloses a synchronization protection circuit, connected to the detection circuit, for performing counting in accordance with the wobble signal, estimating the predetermined period during which the address information is included in the wobble signal, and generating a synchronization protection signal in accordance with the estimated period, the signal selector of the detection circuit providing the PLL circuit with one of the first hold signal, the second hold signal, and the synchronization protection signal (Col. 4, Line 66 – Col. 5, Line 20).

10. Regarding claim 11, Minamino discloses a clock generating device for generating a clock signal synchronizing with a wobble signal that includes address information

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during a predetermined period, wherein the cycle of the wobble signal changes with at least two timings in accordance with the address information of the predetermined period, the clock generating device comprising:

a PLL circuit for generating an oscillation signal in accordance with the difference between the phase of the wobble signal and the phase of the clock signal and for generating the clock signal by synchronizing the oscillation signal with the wobble signal (Col. 8, Lines 45-57);

a monitor, connected to the PLL circuit, for monitoring the wobble signal, wherein the monitor generates a first hold signal that holds the output of the PLL circuit during a first period between a first timing and a second timing, at which the cycle of the wobble signal changes, and a second hold signal that holds the output of the PLL circuit during a second period, which is longer than the first period of the first hold signal measured from the first timing (Col. 17, Lines 10-37); and

a signal detector, connected to the monitor, for providing one of the first and second hold signals to the PLL circuit (Col. 4, Line 66 – Col. 5, Line 20).

Claim Rejections - 35 USC § 103

11. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the

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invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

12. Claims 7-10 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Minamino in view of Katoh (US 6,088,311).

13. Regarding claims 7, 9 and 13, Minamino discloses a phase comparator circuit for generating a phase difference signal in accordance with the difference between the phase of the wobble signal and the phase of the oscillation signal (Col. 1, Lines 25-29; Col. 8, Lines 50-53).

However, Minamino does not disclose but Katoh does disclose a charge pump, connected to the phase comparator, for generating an output signal in accordance with the phase comparator and the charge pump stops functioning in response to one of the first hold signal, the second hold signal, and the synchronization protection signal (Col. 14, Lines 6-31).

Therefore it would have been obvious to one ordinarily skilled in the art at the time of the invention to supplement the teachings of Minamino and have a charge pump, connected to the phase comparator, for generating an output signal in accordance with the phase comparator and the charge pump stops functioning in response to one of the first hold signal, the second hold signal, and the synchronization protection signal, as disclosed by Katoh, in order to control the gain of the PLL circuit according to the frequency of the input data.

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14. Regarding claims 8 and 10, Minamino does not explicitly disclose but Katoh does disclose a frequency divider, connected to the phase comparator, for generating a divisional signal by dividing the oscillation signal by a predetermined dividing ratio, and providing the divisional signal to the phase comparator, the dividing ratio being changed in accordance with the cycle of the wobble signal (Col. 8, Lines 37-46).

Therefore it would have been obvious to one ordinarily skilled in the art at the time of the invention to supplement the teachings of Minamino, and have a frequency divider, connected to the phase comparator, oscillation signal by a predetermined dividing ratio, and providing the divisional signal to the phase comparator, the dividing ratio being changed in accordance with the cycle of the wobble signal, in order to stabilize the loop gain of the PLL channel.

Conclusion

15. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Konishi (US 6,104,682) discloses a disk apparatus having a data reproducing system using a digital PLL.

Maekawa (US 6,606,286) discloses a track loss signal generating apparatus used in an optical disc drive equipped with amplitude adjusting apparatus for a tracking error signal.

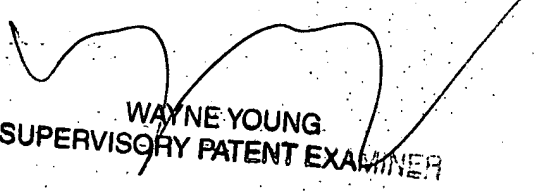
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16. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Minerva Rivero whose telephone number is (571) 272-7626. The examiner can normally be reached on Monday-Friday 9:00 am - 6:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wayne Young can be reached on (571) 272-7582. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

MR 12/5/06


WAYNE YOUNG
SUPERVISORY PATENT EXAMINER